

**Amendments to the Claims:**

The listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A ~~semiconductor memory apparatus~~ method for storing data by accumulating charges in a capacitor, wherein comprising:

before performing a precharge for bringing the potential of a pair of bit lines to an intermediate potential by making a short circuit in the pair of bit lines, the potential of the bit line being charged to a higher level is previously lowered to a level within the range that prevents data written in a memory cell from being disappeared

lowering a potential of a first bit line of a pair of bit lines to a level within a range that prevents data in a memory cell from being lost; and

making a short circuit between said pair of bit lines to perform a precharge of said pair of bit lines by bringing the potential of said pair of bit lines to an intermediate potential,

wherein said short circuit is made after said lowering occurs.

2. (Currently Amended) A semiconductor memory apparatus for storing data by accumulating charges in a capacitor, comprising:

a forced step-down circuit comprised of comprising a first switching element having one end connected to a driving line on the high side, and

a forced step-down capacitor and a second switching element arranged in parallel between the other end of the first switching element and a ground potential, and

a pair of bit lines, wherein a first bit line of said pair of bit lines is connected to said driving line, wherein

the second switching element is brought into an on state in advance to hold the forced step-down capacitor at zero potential before the first switching element is brought into an on state, and

before making a short circuit in the pair of bit lines to perform performing a precharge for by bringing a potential of a pair of bit lines to an intermediate potential by making a short circuit in the pair of bit lines, the first switching element is then brought into an on state to lower and a potential of the driving line on the high side is previously lowered to a level within the a range that prevents of preventing data written in a memory cell from being lost disappeared.

3. (New) A method for storing data in a semiconductor memory apparatus by accumulating charges in a capacitor, said semiconductor memory apparatus having a forced step-down circuit comprising:

a first switching element having one end connected to a driving line on the high side,

a forced step-down capacitor and a second switching element arranged in parallel between the other end of the first switching element and a ground potential, and

a pair of bit lines, wherein a first bit line of said pair of bit lines is connected to said driving line, said method comprising:

bringing said second switching element into an on state to hold the forced step-down capacitor at zero potential;

lowering a potential of said first bit line to a level within a range that prevents data in a memory cell from being lost by bringing said first switching element into an on state after bringing said second switching element into an on state; and

making a short circuit between said pair of bit lines to perform a precharge of said pair of bit lines by bringing the potential of said pair of bit lines to an intermediate potential.

4. (New) The method of claim 1, wherein the intermediate potential is less than 1.5 volts.

5. (New) The method of claim 1, wherein the intermediate potential is from about 1 volt to about 1.25 volts.

6. (New) The method of claim 1, wherein the potential of said first bit line is lowered to a potential from about 2.0 volts to about 2.5 volts.

7. (New) The method of claim 1, wherein said range that prevents data in a memory cell from being lost is defined by a threshold voltage associated with the memory cell.

8. (New) The method of claim 1, wherein making a short circuit comprises bringing a switching element connected to both bit lines of said pair of bit lines into an on state.

9. (New) The semiconductor memory apparatus of claim 2, wherein the intermediate potential is less than 1.5 volts.

10. (New) The semiconductor memory apparatus of claim 2, wherein the intermediate potential is from about 1 volt to about 1.25 volts.

11. (New) The semiconductor memory apparatus of claim 2, wherein the potential of said first bit line is lowered to a potential from about 2.0 volts to about 2.5 volts.

12. (New) The semiconductor memory apparatus of claim 2, wherein said range that prevents data in a memory cell from being lost is defined by a threshold voltage associated with the memory cell.

13. (New) The semiconductor memory apparatus of claim 2, wherein making a short circuit comprises bringing a switching element connected to both bit lines of said pair of bit lines into an on state.

14. (New) The method of claim 3, wherein the intermediate potential is less than 1.5 volts.

15. (New) The method of claim 3, wherein the intermediate potential is from about 1 volt to about 1.25 volts.

16. (New) The method of claim 3, wherein the potential of said first bit line is lowered to a potential from about 2.0 volts to about 2.5 volts.

17. (New) The method of claim 3, wherein said range that prevents data in a memory cell from being lost is defined by a threshold voltage associated with the memory cell.

18. (New) The method of claim 3, wherein making a short circuit comprises bringing a switching element connected to both bit lines of said pair of bit lines into an on state.